

WE CLAIM:

1 1. A semiconductor memory formed in a semiconductor
2 integrated circuit comprising:

3 a semiconductor substrate of a first conductivity type
4 which has at least one well region of a second conductivity type;

5 an array of memory cells which are formed in said well
6 region, each cell of said array including a MOS transistor of the
7 first conductivity type and a capacitor;

8 a plurality of data lines which extend over said well region,
9 and each of which is electrically connected to selected ones of said
10 memory cells of said array;

11 a plurality of word lines which extend over said well region,
12 and each of which is electrically connected to gates of the MOS
13 transistors of selected ones of said memory cells of said array; and

14 a plurality of sense amplifiers each of which is coupled to a
15 pair of adjacent ones of said data lines,

16 said each sense amplifier including a pair of first MOS
17 transistors of the first conductivity type which are formed in one
18 well region of the second conductivity type formed in said semicon-
19 ductor substrate, and a pair of second MOS transistors of the
20 second conductivity type which are formed in said semiconductor
21 substrate,

22 wherein each transistor of said pair of first MOS transistors
23 has its gate cross-coupled to the drain of the other transistor of
24 said pair of first MOS transistors, wherein the drain of one of said
25 transistors of said pair of first MOS transistors is electrically

26 connected to one of said pair of data lines and the drain of the
27 other of said transistors of said pair of first MOS transistors is
28 coupled to the other of said pair of data lines,

29 and further wherein each transistor of said pair of said
30 second MOS transistors has its gate cross-coupled to the drain of
31 the other transistor of said pair of second MOS transistors,
32 wherein the drain of one transistor of said pair of second MOS
33 transistors is electrically connected to one of said pair of data lines
34 and the drain of the other of said transistors of said pair of said
35 second MOS transistors is electrically connected to the other of said
36 pair of data lines.

1 2. A semiconductor memory according to claim 1, wherein
2 said first MOS transistors of said each sense amplifier are formed in
3 a well region which is isolated from said well region having said
4 memory cells formed therein.

1 3. A semiconductor memory according to claim 1, wherein
2 said pair of first MOS transistors and said pair of second MOS
3 transistors of said each sense amplifier are respectively arranged on
4 opposite sides of an area in which said array is formed.

1 4. A semiconductor memory according to claim 1, wherein
2 said plurality of data lines extend along rows substantially in
3 parallel to one another, while said plurality of word lines extend
4 along columns in a direction substantially orthogonal to said data
5 lines.

1 5. A semiconductor memory according to claim 4, wherein
2 said pair of first MOS transistors and said pair of second MOS
3 transistors of said each sense amplifier are respectively located at
4 opposite terminal ends of said pair of data lines.

1 6. A semiconductor memory according to claim 4, wherein
2 said word lines are made of the same material as that of the gates
3 of the MOS transistors of the memory array, and said data lines
4 are made of a metal material and cross over said word lines.

1 7. A semiconductor memory according to claim 6, wherein
2 said data lines are made of aluminum.

1 8. A semiconductor memory according to claim 1, wherein
2 said well region is an epitaxial region.

1 9. A semiconductor memory according to claim 4, wherein
2 a wiring for biasing said well region having said array formed
3 therein is arranged in parallel with said data lines.

1 10. A semiconductor memory according to claim 1, further
2 comprising means coupled to the sources of the pair of first MOS
3 transistors and the pair of second MOS transistors to control a
4 positive feedback operation between the respective cross-coupled
5 transistors of both of said transistor pairs.

1 11. A semiconductor memory according to claim 10, further
2 comprising means for applying a control signal to said positive
3 feedback operation control means to start the positive feedback opera-
4 tion in the pair of first MOS transistors at a time different than the
5 start of the positive feedback operation in the pair of second MOS
6 transistors.

1 12. A semiconductor memory according to claim 1, further
2 comprising a plurality of dummy cells formed in said well region,
3 each of said dummy cells including a MOS transistor, and a pair of
4 dummy word lines which extend over said well region, wherein each
5 of said dummy word lines is electrically connected to gates of the
6 MOS transistors of selected ones of said dummy cells, and further
7 wherein each said dummy cell is electrically connected to a selected
8 one of the plurality of data lines.

1 13. A semiconductor memory according to claim 4, wherein
2 said memory arrangement is divided into two groups of memory cells,
3 each of said groups being coupled to a plurality of data lines and
4 intersecting word lines, wherein the data lines which are coupled to
5 each of said groups are also coupled to a column decoder interposed
6 between the two groups of memory cells for selecting predetermined
7 data lines in said respective groups of memory cells in accordance
8 with address signals received by the column decoder.

1 14. A semiconductor memory according to claim 13, wherein
2 said pair of first MOS transistors and said pair of second MOS tran-
3 sistors of each sense amplifier are respectively located at opposite
4 terminal ends of the data lines coupled to each group of memory cells
5 such that one of said groups of memory cells is interposed between
6 a plurality of said pairs of first MOS transistors and said column
7 decoder and the other of said groups of memory cells is interposed
8 between a plurality of said pairs of second MOS transistors and said
9 column decoder.

1 15. A semiconductor memory according to claim 1, 2, 3, 4,
2 5, 6, 7, 8, 9, 10, 11, 12, 13 or 14, wherein the first conductivity
3 type is the P-type, and the second conductivity type is the N-type.

1 16. A dynamic type semiconductor memory comprising:
2 a plurality of pairs of data lines to which memory cells are -
3 connected;
4 differential amplifiers, each of which amplifies a difference
5 between signal magnitudes appearing on each corresponding pair of
6 data lines,
7 said each differential amplifier including a pair of P-channel
8 MOSFETs which have a drain and a gate of one cross-coupled to a
9 gate and a drain of the other respectively and which have the
10 drains connected to the corresponding pair of data lines respectively,
11 a pair of N-channel MOSFETs which have a drain and a gate of one
12 cross-coupled to a gate and a drain of the other and which have the

13 drains connected to the corresponding pair of data lines respectively,
14 and a circuit which controls positive feedback operations between the
15 respective cross-coupled FETs of both FET pairs;

16 a plurality of word lines, each of which is arranged in a
17 manner to intersect with both of the pair of data lines; and

18 a precharging circuit which sets said respective pairs of data
19 lines at a potential intermediate between two potentials representative
20 of binary signals to be stored in said memory cells prior to the start
21 of positive feedback operations by said positive feedback operation
22 control circuit.

1 17. A dynamic type semiconductor memory according to
2 claim 16, further comprising means for applying control signals to
3 said positive feedback operation control circuit to start the positive
4 feedback operation of the P-channel FET pair and that of the
5 N-channel FET pair at different times.

1 18. A dynamic type semiconductor memory according to
2 claim 17, wherein said circuit for controlling the positive feedback
3 operation of each of said differential amplifiers comprises a P-channel
4 control MOSFET coupled to the sources of said pair of P-channel
5 MOSFETs and an N-channel control MOSFET coupled to the sources of
6 said pair of N-channel MOSFETs, wherein said control signals are
7 coupled to the respective gates of said P-channel control MOSFET and
8 said N-channel control MOSFET to start the respective feedback opera-
9 tions of said pair of P-channel MOSFETs and said pair of N-channel
10 MOSFETs.

1 19. A dynamic type semiconductor memory according to
2 claim 16, wherein said precharging circuit comprises a plurality of
3 N-channel precharging MOSFETs having their sources and drains
4 coupled in series between a precharging voltage source and said
5 respective pairs of data lines and their gates coupled to receive a
6 precharging control signal to turn on said N-channel precharging
7 MOSFETs to couple said precharging voltage source to said data
8 lines, wherein the threshold voltage of said N-channel precharging
9 MOSFETs is less than the threshold voltage of said pair of
10 N-channel MOSFETs of said differential amplifier.

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